Efficient Power Management Strategy of FPGAs Using a Novel Placement Technique

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Abstract — Power consumption is one of the major headaches, which should be tackled by the designers. Also, the parameters that affect significantly the performance and power are the Configurable Logic Blocks (CLBs) and the interconnection components. A novel approach for efficient implementation of applications onto reconfigurable architectures is introduced. The main goal of this technique is to spread out the power consumption across the whole device, as well as to minimize it, achieving a more uniform power consumption map across the whole FPGA. This approach is based on finding the optimal CLB placement according to resource utilization map. The proposed methodology can be applied for mapping applications with an efficient power management strategy. Furthermore, the proposed placement algorithm reduces the total power consumption, the leakage power, the total energy and silicon area. The proposed methodology is fully-supported by the software tool called EX-VPR. The result of applying this placement strategy is the power consumption reduction about 5%, while we distribute the power consumption with a rather "uniformly" fashion across the whole device minimizing the power spikes.

I. INTRODUCTION

A Field-Programmable Gate Array (FPGA) is an integrated circuit that can include thousands of identical, programmable logic cells. A matrix of wires and programmable switches interconnects individual logic cells. A typical design involves specifying the simple logic function for each cell and selectively closing the switches in the interconnect matrix. To operate properly, the FPGA must employ appropriate power-management technology. FPGA power consumption depends on the requirements of internal circuits, which are: (i) the configurable logic block (CLB), (ii) the I/O blocks (IOB), and (iii) the interconnection wires. In particular, a CLB provides the functional logic elements, while an IOB provides the interface between the package pins and internal signal lines. The programmable interconnect resources provide the routing paths to connect the inputs and outputs of the CLBs and IOBs onto the appropriate networks. So, an efficient power management strategy should handle wisely all these controversial parameters and manipulate effectively the available hardware resources.

Several approaches for designing low-energy and/or high-performance FPGAs by optimizing the interconnection architecture has been reported [8], [12], [13], [11], [10], [9], [4], [3]. Among others, the design of non-homogeneous interconnection structure [13], [11], [4] and the use of multiple supply voltages, $V_{DD}$, and/or multiple threshold voltages [10], [9], [3] were the main strategies, which have been chosen for achieving optimal FPGA designs.

Due to the fact that about 60% of an FPGA power is occupied by routing resources [4], the researchers have spent much effort on minimizing power leading to smaller devices, achieving higher frequencies and consuming less energy. Implementing FPGAs in deep-submicron technology (<0.13µm), the leakage power became a dominant power component with equal importance with the dynamic power consumption. Thus, we study the relation of both the total energy consumption and the leakage power associated with the routing components.

The goal of the proposed technique is to achieve a better power management strategy. In other words, we solve the following problem: Given a certain power budget of an application implemented into FPGA architecture, find an appropriate mapping of the same application onto similar FPGA hardware resources, which re-distributes the power budget over the whole FPGA device into one more “balanced” way, reducing the number and amplitude of the power consumption peaks. The proposed approach is based on finding out the optimal placement for the logic elements of an island style-based FPGA platform, taking into account the considered application-domain characteristics. The efficiency of an application mapping is characterized by analyzing parameters such as power dissipation, performance, and the minimum number of required routing tracks. We made an exhaustive exploration with all the kinds of MCNC benchmarks (i.e. combinatorial, sequential and FSM), to find out spatial information from hardware resources.

As the modern reconfigurable devices consume more power compared to ASIC solutions, the researchers spent effort to tackle this issue. One of the most important defects of the power is the heat that produced within the
As this heat increases, a number of problems that affect the final application implementation occur. Among them, the reliability of the system, the packaging of the chip and the lifecycle of the final product are some critical issues. Moreover, as the FPGA power consumption continues to increase, low-power FPGA circuitry, architectures, and CAD tools need to be developed. The second part of the paper is focused on a novel placement algorithm development which uses as cost function a trade-off among power consumption, leakage power, total energy, maximum frequency and area. The methodology is based on finding the optimal CLB placement according to resource utilization map. The main goal of this placement is to minimize the total power consumption as well as to spread it across the whole FPGA device.

The paper is organized as follows. In Section 2, the proposed methodology for implementing FPGA interconnection architecture composed by longer segment wires and multiple SBs as well as the power-aware placement is introduced. Section 3 presents the comparison results, while conclusions are summarized in Section 4.

II. THE METHODOLOGY FOR EFFICIENT MAPPING APPLICATIONS ONTO FPGAS

In this section, we discuss the spatial information extracted from the hardware resources. Due to the fact that we are working on reconfigurable architectures, we target to routing resources (SB connections and the usage of longer segments) as well as the CLBs and their impact on the FPGA performance. For that purpose, we introduce a new method for deriving special maps, each of which describes the number, as well as the location (spatial) of used hardware resources across the whole device. In order to build these maps, MCNC benchmarks, the EX-VPR tool [2] and a Virtex-like FPGA architecture [7] were used.

The proposed strategy for the efficient power management in an FPGA consists of two steps (Fig.1). Detailed description of every step of the developed methodology, as well as its evaluation, will be given in the forthcoming sections. Furthermore, the methodology is software-supported by a new tool named EX-VPR. The tool is based on VPR [1], [5], and it is part of the MEANDER framework [6]. Extensive description of the whole design framework can be found in [2].

A. Visualization of Spatial Information

The first step of the methodology is to find out the performance, the power consumption, the connectivity and the area requirements of MCNC benchmarks. Particularly, by the term connectivity we define the total number of active connections, i.e. the “ON” pass-transistors, which take place into a SB. A specific map (or set of curves) can be created for each aforementioned design parameter, which shows the parameter variation across (X,Y)-plane of the whole FPGA device.

Fig. 2 shows the average connectivity of all kinds of MCNC benchmarks of the whole FPGA, in normalized manner. Similar 3-D graphs can be derived for any application-domain specific benchmarks or applications. It can be seen that the connectivity changes from point to point of FPGA and the number of used pass-transistors (i.e. ‘ON’ connections) decreases gradually from the center of FPGA architecture to the I/O blocks. The connectivity requirement for more tracks in the center of the device, compared to the borders depends on the chosen routing algorithm [5] and therefore, the interconnection resources are not utilized uniformly over any (x,y) point of FPGA. Consequently, the challenge which should be tackled by a designer is to choose only the needed hardware resources, considering the associated spatial information from the connectivity distribution graph. The connectivity degree of (x,y) point of FPGA array is straightforward-related with the power consumption of (x,y) SB location, since less number of active SB connections means smaller capacitance and thus, less power consumption. Thus, employing the appropriate amount of hardware, significant total power consumption, leakage power, power dissipation, silicon area and delay reduction can be achieved.

The power consumption map is very useful instrument to FPGA device designers to specify the power consumption over each (x,y) point of FPGA device. Determining the “hot spots” locations of FPGA device, the designer can concentrate his/her efforts for the reducing power consumption on certain regions only, but not on the whole device, reducing the design-time costs and alleviating the time-to-market pressure. Comparing the connectivity graph (Fig. 2) with the power dissipation graph
(Fig. 3), it can be easily concluded that the corresponding graphs are quite similar due to the proportional relationship between the connectivity degree and the power consumption.

1. Performing exploration with all MCNC benchmarks, which are combinatorial, sequential, and FSM circuits, the derived 3-D graph provides a global view to (almost) all possible applications, which can be mapped on a FPGA. Therefore, the proposed FPGA architecture with different routing features can be considered as a general-purpose FPGA platform.

2. Visualizing the spatial information of a certain application domain, for instance, DSP applications, block matching (or video compression) algorithm, we can derive an application-specific FPGA platform which is specialized and optimized under the specific constraints of the considered application-domain.

3. Depending on the fabrication costs and the volume number of chips, the proposed methodology may be used for the description of a FPGA architecture optimized for a specific application only, for instance, MPEG-2. This option might be considered as an alternative solution to Structured-ASICs.

In this paper, we provide comparison results assuming the FPGA architecture as a general-purpose platform (i.e. option (a)). The next sections describe the proposed placement algorithm for efficient mapping of applications onto reconfigurable architectures taking into consideration the power dissipation across the whole device.

B. The Proposed Power-Aware Placement Approach

In this section, a novel algorithm for power-aware placement for FPGA architectures is introduced. This technique tries to minimize the total power consumption, the leakage power as well as the silicon area with the minimal impact on the frequency operation. Taking into consideration that the thermal effect is function of the total power consumption of the FPGA, the minimization of the power that consumed by the device will lead to heat reduction. In other words, this approach may be used as a heat management technique. The basic idea behind the proposed placement algorithm is to prohibit mapping movement of CLBs from the center to the FPGA (where the most power consumption is spent) to the rest device. Based on the visualization results from the first step of the methodology (Fig. 2 and Fig. 3), we can deduct that there is a need for higher connectivity into the center of the device compared to the corners. As the connectivity factor is proportional to the power consumption and to the heat that produced by the chip, we can deduct that the center of the FPGA is more critical compared to the corners for minimizing all these design parameters.

The proposed technique aims at the power, leakage, power and required area minimization, taking into account the number of CLBs that are not utilized across the FPGA. Due to the fact that the EX-VPR tool tries to find out the minimal square FPGA that fits the application, a number of
CLBs may be left inactive after the placement and routing procedure. For instance, if we have an application that requires 82 CLBs, the EX-VRP tool reports that it maps the application onto a 10x10 array (the smallest square array that fits the application). In such a case, a number of 18 CLBs are inactive in the FPGA. After the simulated annealing-based placement and routing procedure, the final picture of the application will be similar to Fig. 4(a). Here, almost all of the inactive CLBs are placed onto the corners of the device. If we compare the Fig. 4(a) with the Fig. 2 we can deduce that the center of the device is crowded by active CLBs and routing tracks, while the hardware resources at the corners are under utilized. This non-uniformity in hardware utilization across the device leads to different power consumption at different FPGA regions.

In our approach (Fig. 4(b)), we try to reduce the power consumption onto the center of the device, which leads to more uniform power dissipation across the whole FPGA. In addition to that, with our placement algorithm we achieve to reduce the temperature at the center of the device. The main goal of our methodology is to draw away resources from the center of the device. Due to the fact that we can not move SBs and routing tracks (because these affect the final routing), we have to move CLBs. By routing the power-aware placement, the routing resources are utilized in a more “balanced” manner across the whole device.

As the logic functions of CLBs are moved from the center to the periphery, the power consumption (and the heat dissipation of the device) is spread across the whole FPGA. The result of this power-aware placement algorithm is an application mapped onto a reconfigurable architecture, where the available CLBs in the periphery are fully-utilized, while on the center are no. Also, the interconnection network in the center is utilized in a more uniform manner compared to corners. Taking in consideration that the total power (and heat) is proportional to the active hardware resources (logic and interconnection), this algorithm separates these two components by leaving into the center of the device only the required routing and at the corners the active CLBs.

The proposed efficient placement strategy was implemented and tested by a number of MCNC benchmarks. The chosen MCNC benchmarks are the twenty largest ones, and they were placed and routed in an island-style FPGA array [6, 8] implemented in a 0.18µm TSMC CMOS process, using the EX-VPR tool. All the benchmarks were mapped to the smallest FPGA array. The
results are shown in Table 1. The average gain in total power consumption is about 5%. Similar results can be achieved for leakage power (2%) and energy consumption (2%). The penalty in maximum frequency is about 1%. It can be deduced that this method minimizes all the parameters that affect the total power consumption of the reconfigurable architecture. However, the most important consequence the proposed approach is that the fact that spreads both the power and the heat produced across the whole device leading to better packaging solutions.

The comparison between the traditional placement approach and the proposed power-efficient placement is shown in Fig. 5. Both approaches are based on the simulated annealing algorithm, taking into account the locations of the non-utilized CLBs for the latter one. It can be seen that the proposed technique minimizes the total power consumption across the whole device and reduces the power consumption spikes. The latter characteristic allows more “uniform” power consumption and eventually, more “uniform” heat distribution across an FPGA device.

Projecting the 3-D curves of Fig. 5(a) and (b), we derive the corresponding maps shown in Fig. 6 (a) and (b), which show the heat variations of the device for each (x,y) point of the FPGA. It is apparent that the proposed power-aware placement algorithm achieves both the heat distribution in a rather uniform way across the whole device and the minimization of the maximal values of heat.

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### IV. CONCLUSIONS

A novel methodology for efficient designing and implementing applications onto island-style FPGA architectures was presented. The approach is based on the appropriately usage of the spatial information of various FPGA parameters. The proposed techniques achieve both power reduction and more uniform distribution across the whole device. In particular, the exploration for the power-aware placement gave very promising results. We proved that the designer can re-distribute a certain amount of the power over the hardware resources, resulting into a “balanced” power consumption profile. In addition to, we achieved about 5% savings in total power consumption. Due to the proportional relation between power and heat dissipation, the proposed power management strategy gives better solutions for packaging, performance and reliability of the reconfigurable architectures. Furthermore, we achieve area reduction about 2%, leading to smaller devices. Finally, the methodology is fully software-supported by the tool EX-VPR.
Figure 6. Thermal distribution after P&R procedure: (a) the existing placement approach in VPR and (b) the proposed power-aware placement approach.

V. REFERENCES